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09/934,099	08/21/2001	David Alexander Grant	TI-33249	7892

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/934,099	Applicant(s) GRANT ET AL.	
	Examiner Tse Chen	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 3, 6, 7, 13, 18, and 30 are objected to because of the following informalities:

- As per claim 3, "upon an *in* initialization" should be corrected to "upon an initialization";
- As per claim 6, "circuit outputs" should be "circuits output" in order to avoid ambiguity problem related to first or second circuit and "when *a* continuously clocked" should be corrected to "when continuously clocked";
- As per claim 7, "circuit comprise" should be "circuit comprises";
- As per claim 13, "circuit have" should be "circuit has";
- As per claim 18, "comprising the steps of" should be "comprising the step of" as there is only one step; and
- As per claim 30, "thepower" should be "the power".

Appropriate correction is required.

Findings

2. The rejections in this Office Action are supported by the following findings:

3. Boudry et al., U.S. Patent 5305453, hereinafter Boudry, discloses:

3.1. A synchronized sampled data system [col.1, ll.6-8].

3.2. The synchronized sampled data system comprising a shared data bus [CMB] providing an instructional word [command] [col.4, ll.37-43; col.5, ll.61-67].

3.3. The synchronized sampled data system comprising a first sampled data circuit [memory card MU #1] and a second sampled data circuit [MU #2] each receiving the instructional word on the shared data bus [col.4, ll.7-12, ll.22-25; col.5, ll.61-67].

3.4. Each said first circuit and said second circuit having an output phase [CLK1 or CLK2] as a function of at least one control signal [RE] provided to each said circuit via said shared data bus [col.4, ll.44-49; col.7, ll.44-56].

3.5. A different predetermine start count [value RF] is preloaded into each of the first circuit and the second circuit upon an initialization of the sampled data system [col.5, ll.36-41; col.6, ll.37-40; different manufacturing processes yield different values].

3.6. Each said first and second circuit comprises a power converter [amplifier CIB].

3.7. Each said power converter has multiple outputs [modules M1-M5] each being phase shifted with respect to the outputs of the other power converter [col.7, l.67-col.8, l.8; vary validation signal to produce shifted outputs].

3.8. Each said first and second circuit has a plurality N of common control signals [col.4, ll.47-49].

3.9. The synchronized sampled data system comprising a total of 2^N sampled data circuits, where N is 2 or greater [fig.1] [e.g., N=2, then 4 sampled data circuits of CPU, IOU, SCU and MU].

4. Takeuchi et al., U.S. Patent 4345241, hereinafter Takeuchi, discloses:

4.1. A synchronized sampled data system [fig.3; col.1, ll.26-29; col.5, ll.13-21].

4.2. The synchronized sampled data system comprising a first sampled data circuit [ADC 4] and a second sampled data circuit [ADC 6].

4.3. Each said first circuit and said second circuit having an output phase shifted from the other as a function of at least one control signal [clock signals a1 and a2] provided to each said circuit [col.3, ll.42-46].

4.4. Each said first and second circuit [ADC] comprises an A to D converter.

4.5. The advantage of having output phases shifted for multiple sampled data circuits is the increase in resolution of the sampling frequency [col.1, ll.29-31; col.2, ll.18-22].

5. Jones et al., U.S. Patent 4004099, hereinafter Jones, discloses:

5.1. A synchronized sampled data system [col.1, ll.48-59; calls are connected when their designated time slots are synchronized].

5.2. The synchronized sampled data system comprising a first sampled data circuit and a second sampled data circuit [sampling circuits 14; fig.1].

5.3. Each said first circuit and said second circuit have a respective counter [circulating shift registers 22; col.2, ll.12-19; clock pulse advances information bit through stages as in a counter].

5.4. Each said counter having a different count [information bit] as a function of a common control signal [write signal 44] [col.2, ll.42-47; different information bit transmitted over line 34 and inputted into register 22 as a function of a common control signal 44].

5.5. Each of the first circuit and second circuit are clocked by a common clock signal [26] to produce the phase shifted outputs [col.2, ll.16-30].

5.6. The phase shift of the outputs [time slot gating signal] being correlated to the difference in counts between the respective counter [col.2, ll.16-30; col.3, ll.57-68; different information bit will have output shifted due to different time to propagate through stage].

5.7. The circuits output continuously maintain the phase shift when continuously clocked by the clock signal [col.2, ll.16-30; col.3, ll.66-68].

5.8. The phase shift between the first and second circuit has a granularity of 1/M clock cycles, where M is the number of clock cycles in a count interval [col.2, ll.14-30; M=1 clock cycle between stages of register 22, then first and second sampling data circuits 14 will have granularity of 1 clock cycle].

6. Losel et al., U.S. Patent 4730125, hereinafter Losel, discloses:

6.1. A synchronized system [col.1, ll.8-10] comprising a first [RS1] and second circuit [RS2].

6.2. Each said first and second circuit comprises a power converter [voltage converter; col.2, ll.52-57].

6.3. The outputs of the first and second circuits are shifted 180 degrees from each other [col.4, ll.7-11].

6.4. The noise generated by each said power converter is staggered [col.1, ll.58-67; col.2, ll.18-34; shifting the output phase staggers and distributes the noise].

6.5. Each said power converter includes an integrator circuit having a value corresponding to a phase of the respective circuit [col.2, l.67-col.3, l.13].

6.6. The noise generated at switching instants of a phase staggered power converter occurs at twice the repetition rate and less current as compared to unstaggered synchronized power converters [col.1, ll.58-67; col.2, ll.18-34; inherently, the noise generated at switching instants of a phase staggered power converter will occur at a multiple of the repetition rate and at less current as compared to an unstaggered converter due to the distribution of the noise component].

7. Other findings:

7.1. The Examiner hereby takes Official Notice that the number of available options [possible values] in a binary system with N control lines is equivalent to 2^N.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Re Claims 1, 3, 7, 11, 13-15, 17-18, 20-21, 23, 25, 27, 31, and 33-34

9. Claims 1, 3, 7, 11, 13-15, 17-18, 20-21, 23, 25, 27, 31, and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boudry in view of Takeuchi.

10. In re claim 1, Boudry discloses each and every limitation of the claim [findings 3.1-3.4], except having the output phases of the circuits shifted from the other. Takeuchi teaches a synchronized sampled data system comprising a first sampled data circuit and a second sampled data circuit each having an output phase shifted from the other as a function of at least one control signal provided to each said circuit [findings 4.1-4.3] in order to increase the resolution of the sampling frequency [finding 4.5]. It would have been obvious to one of ordinary skill in the art, having the teachings of Boudry and Takeuchi before him at the time the invention was made, to modify the system taught by Boudry to include the phase shifting technique as taught by Takeuchi in order to have the output phases of the circuits shifted

from the other. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase the resolution of the sampling frequency.

11. As to claim 3, see finding 3.5.

12. As to claim 7, see finding 3.6.

13. As to claim 11, see finding 3.7.

14. As to claim 13, see finding 3.8.

15. As to claim 14, Boudry discloses binary system [computers are binary machines] with N control signals as discussed in reference to claim 13; therefore, the system will have 2^N available shifts [finding 7.1].

16. As to claim 15, see finding 3.9.

17. As to claim 17, see finding 4.4.

18. As to claim 18, see discussion in reference to claim 1. Boudry and Takeuchi teaches the system; therefore, Boudry and Takeuchi teaches the method of operating the system.

19. As to claim 20, see finding 3.2 [shared bus comprises at least one common signal line].

20. As to claim 21, see discussion in reference to claim 14.

21. As to claim 23, see finding 3.5.

22. As to claim 25, see finding 3.9.

23. As to claim 27, see finding 3.6.

24. As to claim 31, see finding 3.7.

25. As to claim 33, see finding 3.8.

26. As to claim 34, see finding 4.4.

Re Claim 2, 4, 6, 16, 19, 22, 24, and 26

27. Claims 2, 4, 6, 16, 19, 22, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boudry and Takeuchi as applied to claim 1 above, and further in view of Jones.

28. In re claim 2, Boudry and Takeuch discloses each and every limitation of the claim as discussed above in reference to claim 1, except for the circuits having a respective counter with a different count as a function of a common control signal. Jones teaches a synchronized sampled data system comprising a first and a second circuit each having a respective counter having a different count as a function of a common control signal [findings 5.1-5.4] in order to shift the phase of outputs. It would have been obvious to one of ordinary skill in the art, having the teachings of Boudry, Takeuchi and Jones before him at the time the invention was made, to modify the system taught by Boudry and Takeuchi to include the counter as taught by Jones in order to have the output phases of the circuits shifted from each other. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase the resolution of the sampling frequency [finding 4.5].

29. As to claim 4, see findings 5.5-5.6.

30. As to claim 6, see finding 5.7.

31. As to claim 16, see finding 5.8.

32. As to claim 19, see discussion in reference to claim 2.

33. As to claim 22, see finding 5.8.

34. As to claim 24, see findings 5.5-5.6.

35. As to claim 26, see finding 5.7.

Re Claims 5, 8, 9, 10, 12, 28, 29, 30, and 32

36. Claims 5, 8, 9, 10, 12, 28, 29, 30, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boudry and Takeuchi as applied to claims 1 and 7 above, and further in view of Losel.

37. In re claims 5 and 8, Boudry and Takeuchi discloses each and every limitation of the claim as discussed above in reference to claims 1 and 7, except for the circuits having outputs shifted 180 degrees from each other. Losel teaches a synchronized system comprising a first and second circuit wherein the outputs of the first and second circuits are shifted 180 degrees from each other [findings 6.1-6.3] in order to distribute any noise components [finding 6.4]. It would have been obvious to one of ordinary skill in the art, having the teachings of Boudry, Takeuchi and Losel before him at the time the invention was made, to modify the system taught by Boudry and Takeuchi to include the 180 degrees shift as taught by Losel in order to distribute noise components. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to distribute the noise components via the phase shift and thus, increase the signal to noise ratio.

38. As to claim 9, see finding 6.4.

39. As to claim 10, see finding 6.6.

40. As to claim 12, see finding 6.5.

41. As to claim 28, see discussion above in reference to claim 5.

42. As to claim 29, see finding 6.4.

43. As to claim 30, see finding 6.6.

44. As to claim 32, see finding 6.5.

Conclusion

45. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Willes et al., U.S. Publication 2002/0064218, discloses a synchronized communication system with counters.
- Kushner, U.S. Patent 5880689, discloses a sampled data system with digital to analog converters.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (703) 305-8580. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
June 7, 2004

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